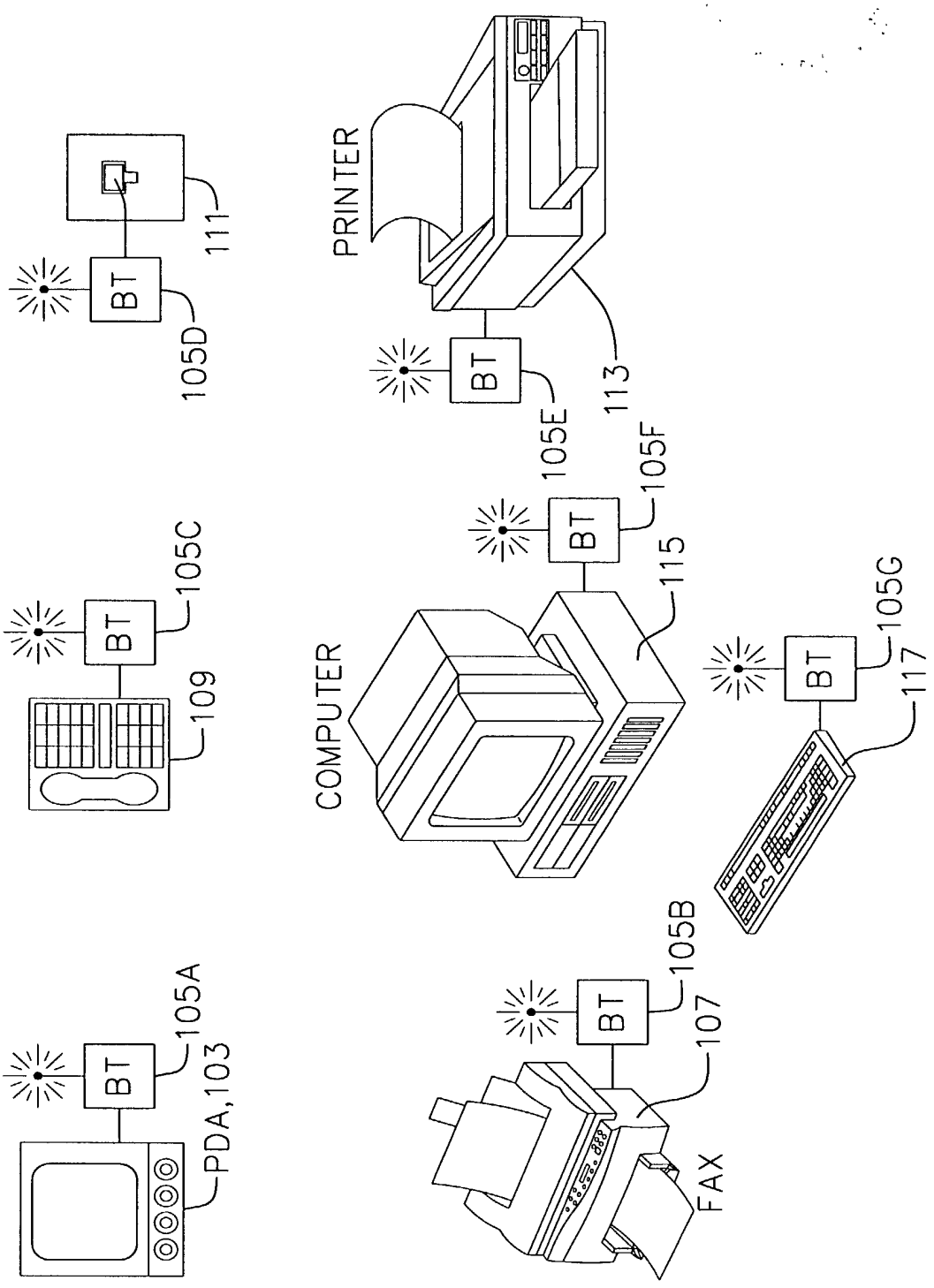
FIG. 1


101
BT
105A
PDA,103
BT
105B
107
FAX
BT
105C
109
BT
105D
111
PRINTER
BT
105E
113
COMPUTER
BT
105F
115
BT
105G
117

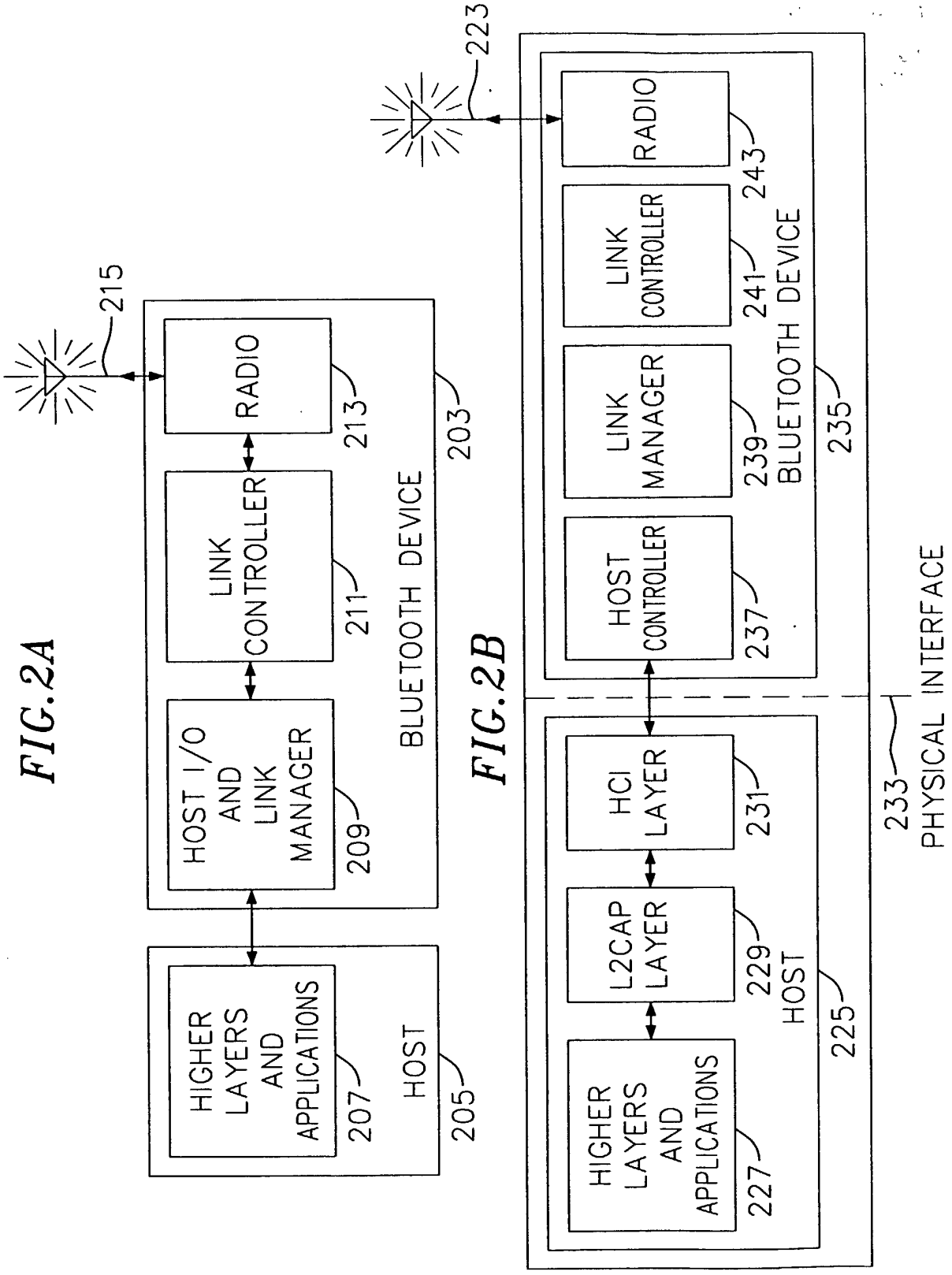

215
RADIO
213
LINK CONTROLLER
211
HOST I/O AND LINK MANAGER
209
BLUETOOTH DEVICE
203
HIGHER LAYERS AND APPLICATIONS
207
HOST
205

FIG.2A

223
RADIO
243
LINK CONTROLLER
241
LINK MANAGER
239
HOST CONTROLLER
237
BLUETOOTH DEVICE
235
HCI LAYER
231
L2CAP LAYER
229
HIGHER LAYERS AND APPLICATIONS
227
HOST
225
233
PHYSICAL INTERFACE

FIG.2B

FIG. 2C

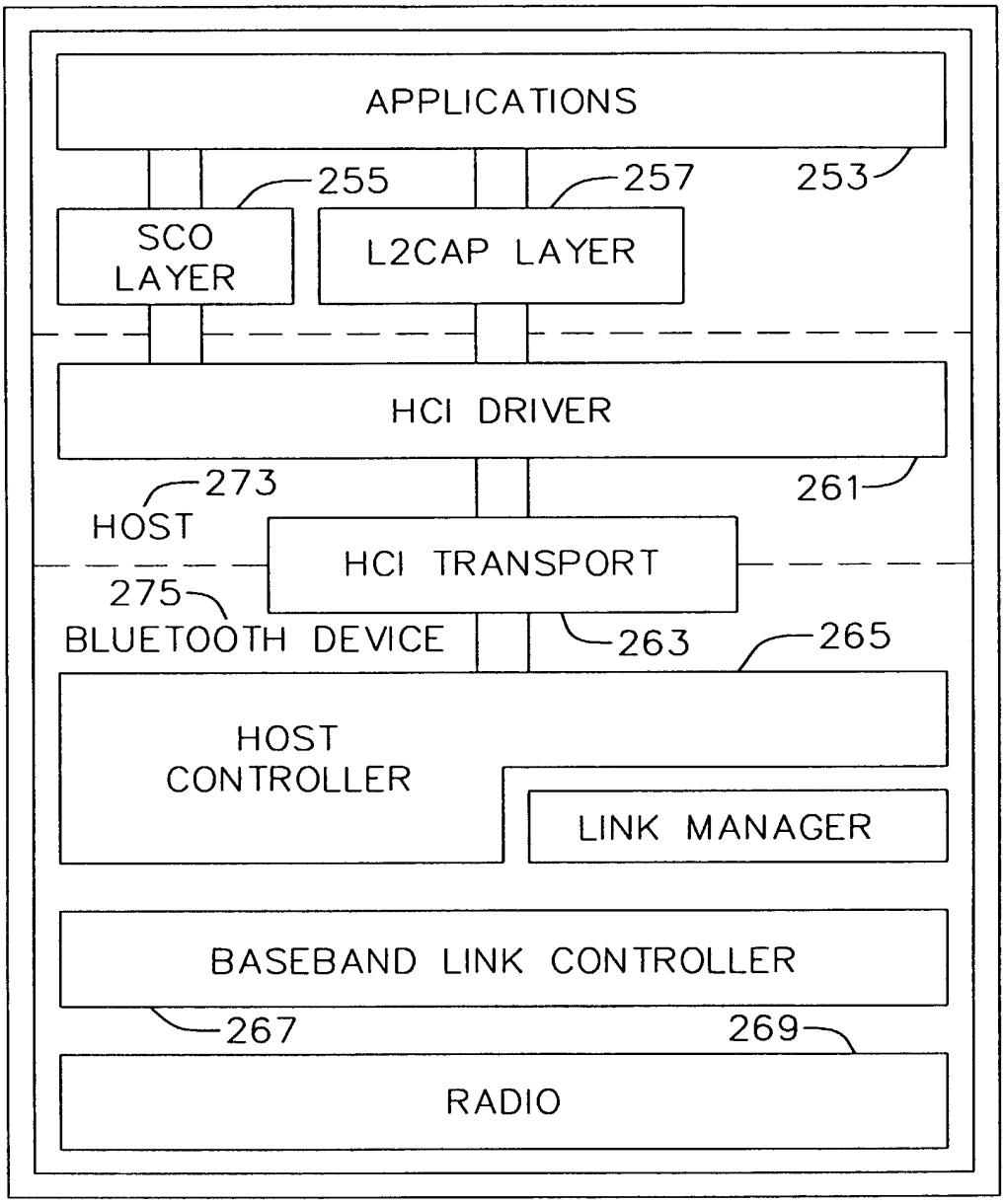

APPLICATIONS
255
257
253
SCO LAYER
L2CAP LAYER
HCI DRIVER
273
261
HOST
HCI TRANSPORT
275
BLUETOOTH DEVICE
263
265
HOST CONTROLLER
LINK MANAGER
BASEBAND LINK CONTROLLER
267
269
RADIO

FIG. 3

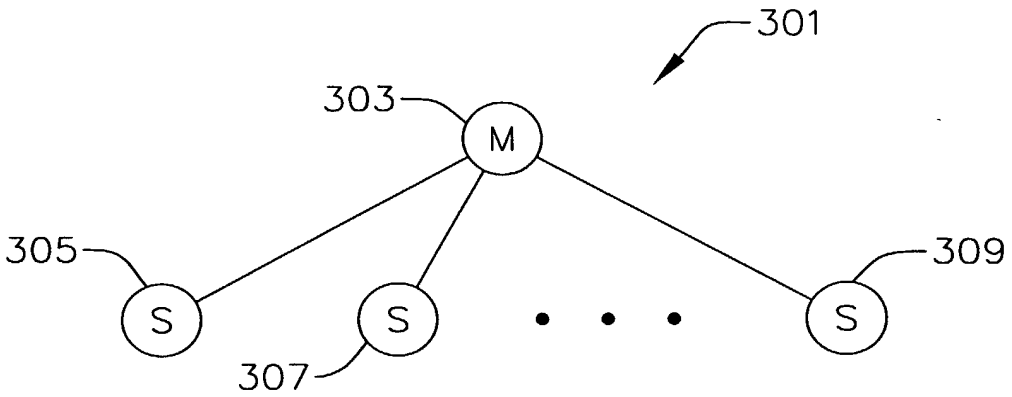

301
303
M
305
309
S
S
S
307

FIG. 4

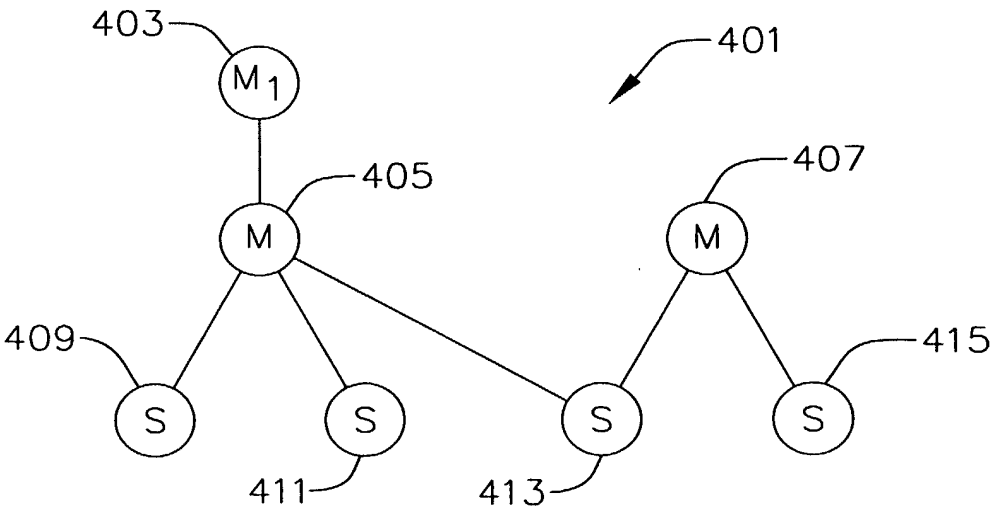

403
M_1
401
405
407
M
M
409
415
S
S
S
S
411
413

FIG.5

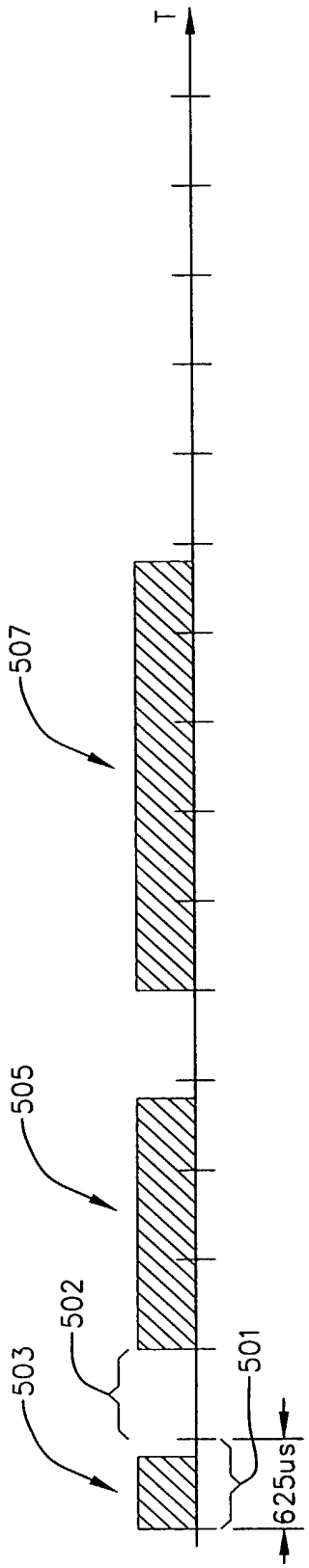


FIG. 6

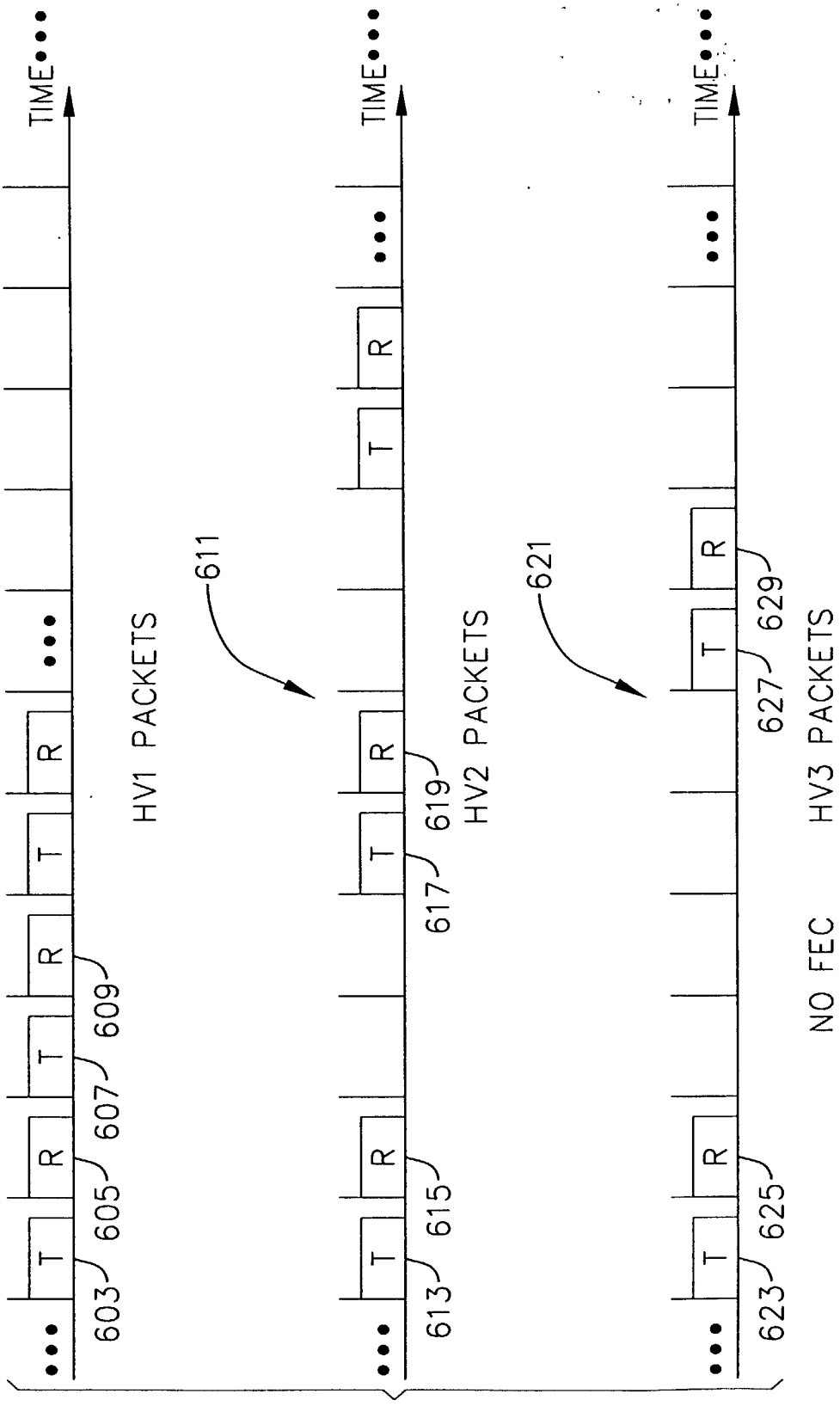

601
TIME
T
R
603
605
607
609
HV1 PACKETS
611
613
615
617
619
HV2 PACKETS
621
623
625
627
629
HV3 PACKETS
NO FEC

FIG. 7

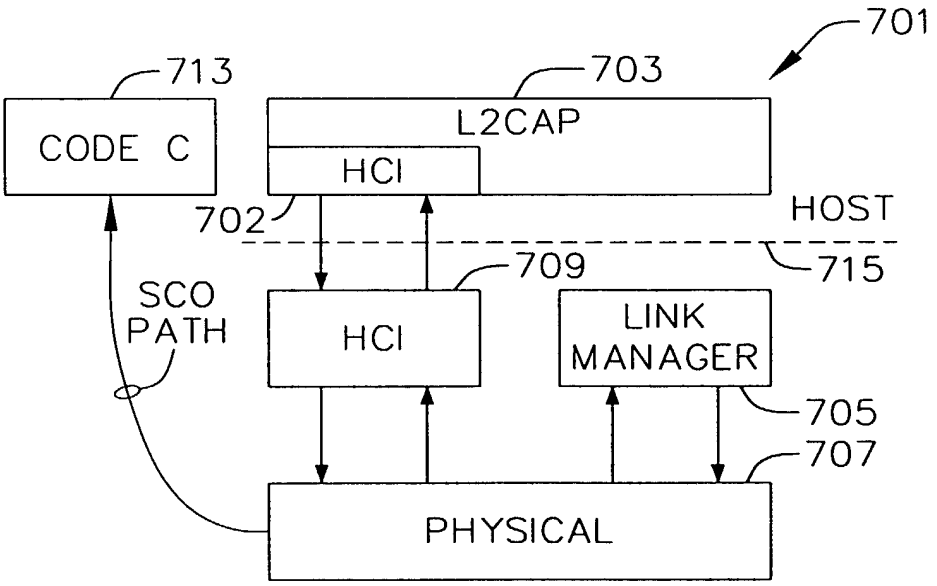

701
713
703
CODE C
L2CAP
HCI
702
HOST
715
709
SCO
PATH
HCI
LINK
MANAGER
705
707
PHYSICAL

FIG. 8

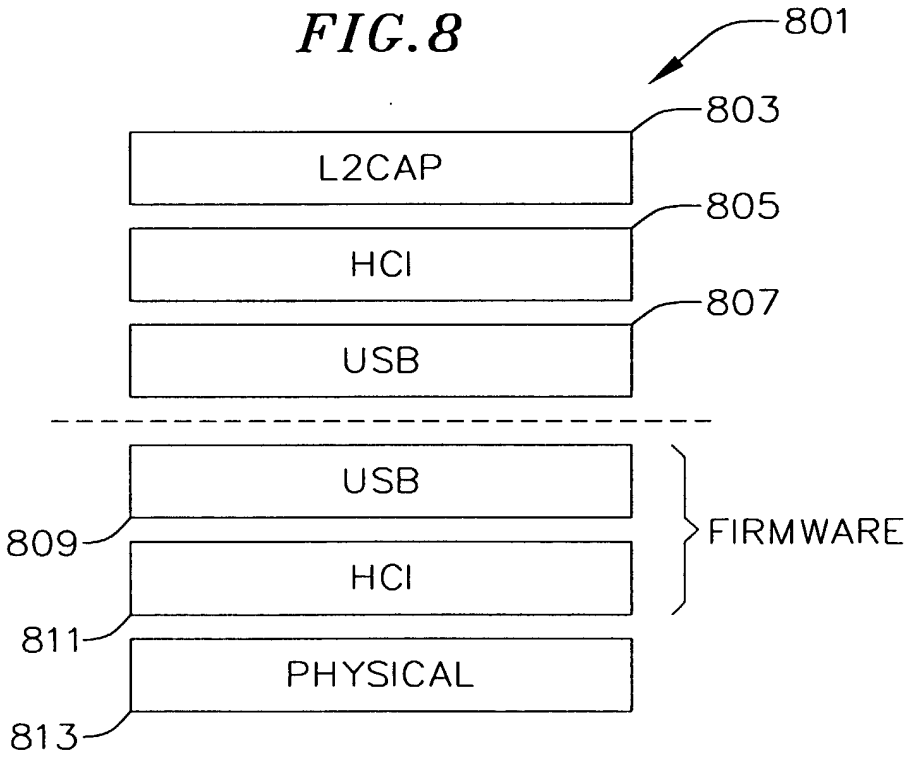

801
803
L2CAP
805
HCI
807
USB
USB
809
FIRMWARE
HCI
811
PHYSICAL
813

FIG. 9

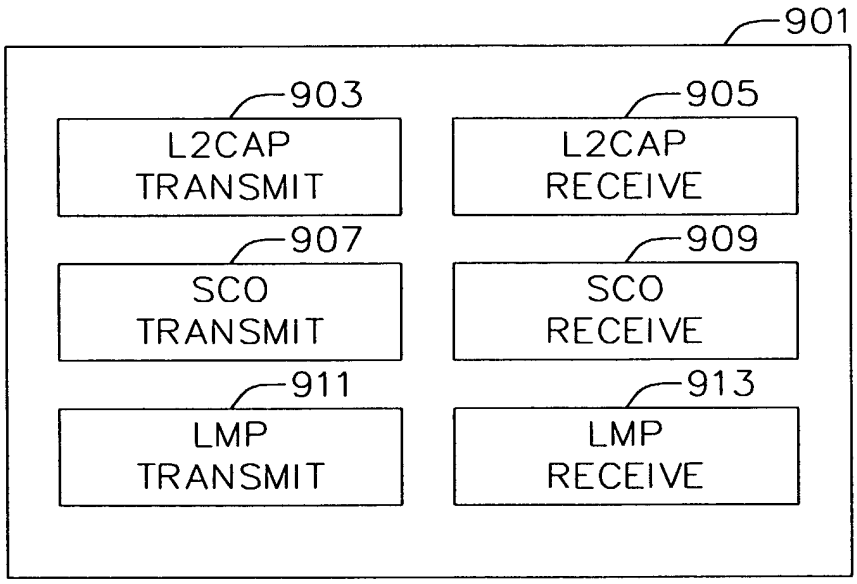

901
903
L2CAP TRANSMIT
905
L2CAP RECEIVE
907
SCO TRANSMIT
909
SCO RECEIVE
911
LMP TRANSMIT
913
LMP RECEIVE

FIG. 10

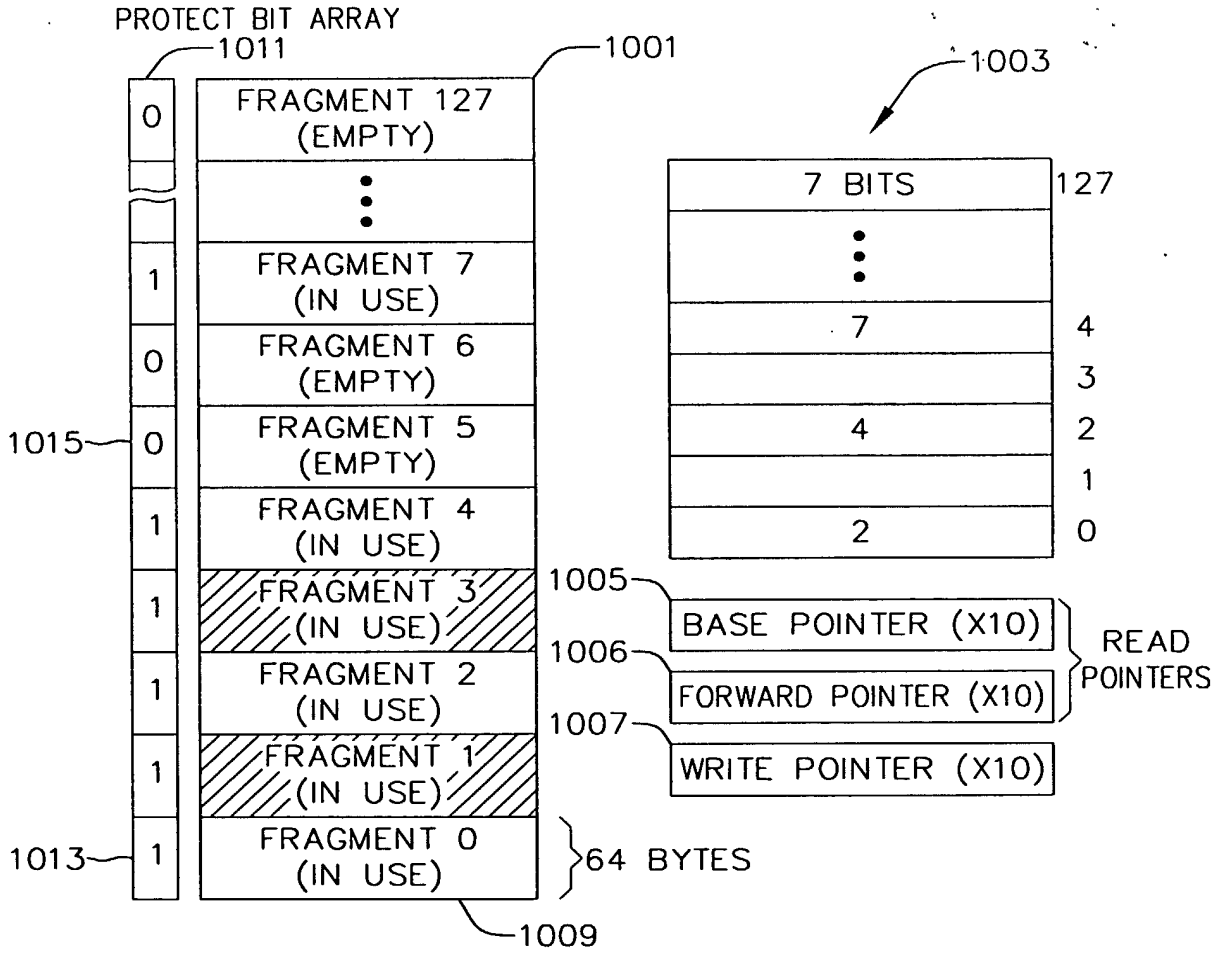

PROTECT BIT ARRAY
1011
1001
1003
0
FRAGMENT 127 (EMPTY)
1
FRAGMENT 7 (IN USE)
0
FRAGMENT 6 (EMPTY)
1015
0
FRAGMENT 5 (EMPTY)
1
FRAGMENT 4 (IN USE)
1
FRAGMENT 3 (IN USE)
1
FRAGMENT 2 (IN USE)
1
FRAGMENT 1 (IN USE)
1013
1
FRAGMENT 0 (IN USE)
64 BYTES
1009
7 BITS
127
7
4
3
4
2
1
2
0
1005
BASE POINTER (X10)
1006
FORWARD POINTER (X10)
READ POINTERS
1007
WRITE POINTER (X10)

FIG. 11

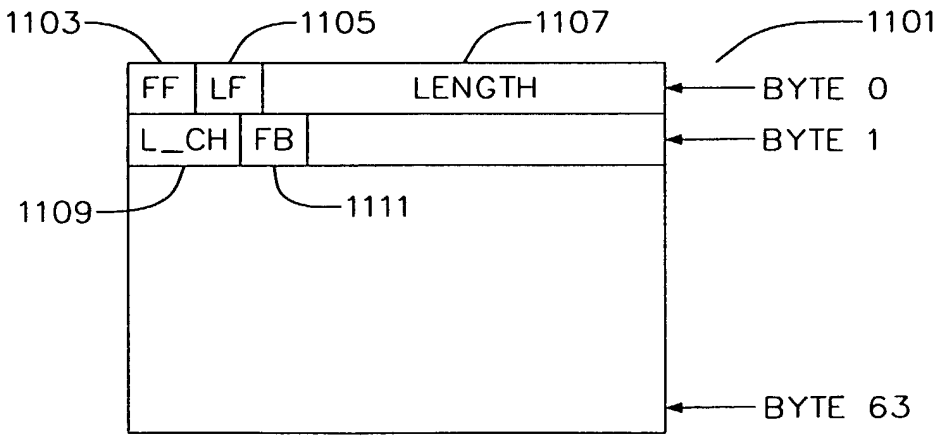

1103
1105
1107
1101
FF
LF
LENGTH
BYTE 0
L_CH
FB
BYTE 1
1109
1111
BYTE 63

FIG. 12

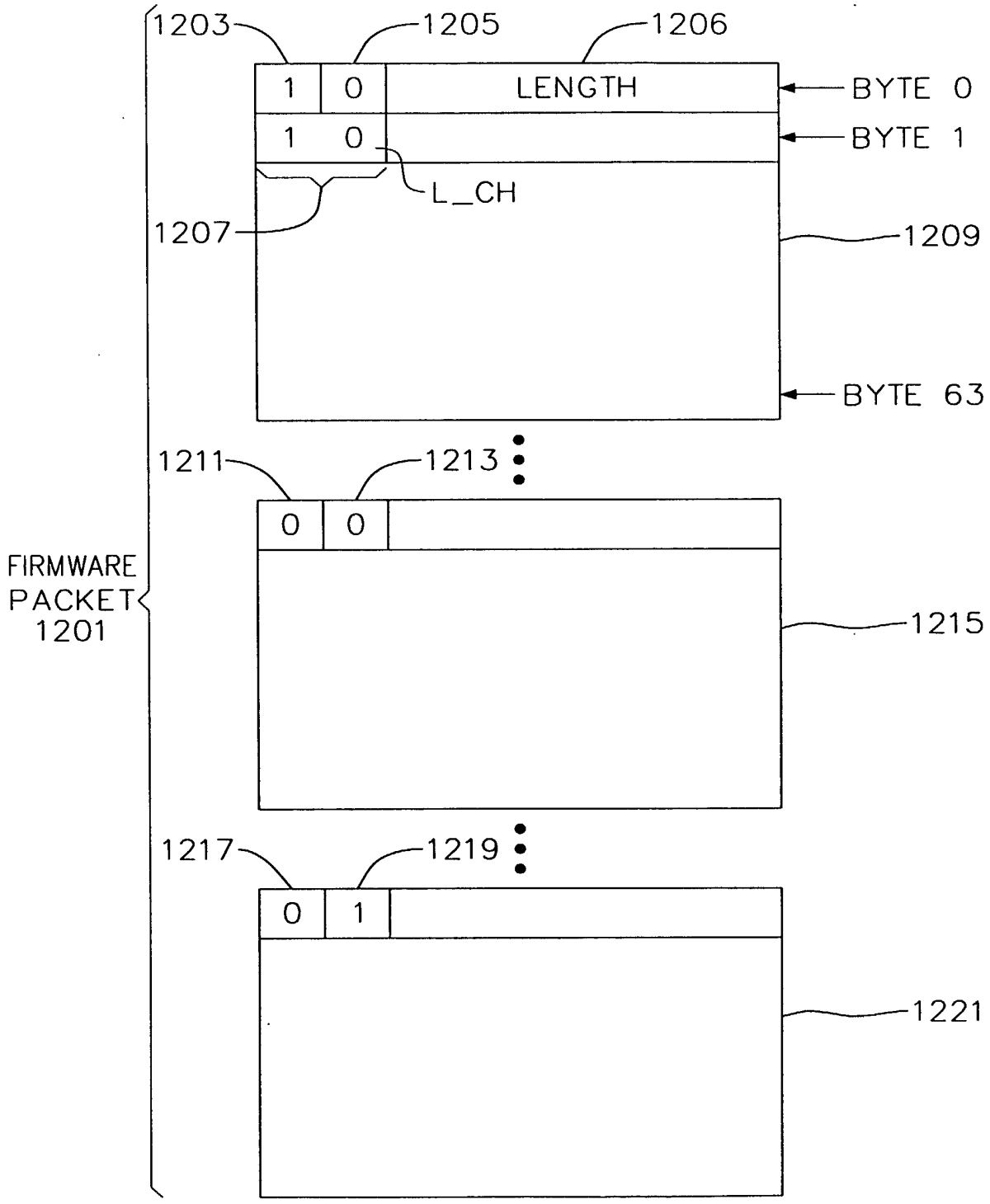
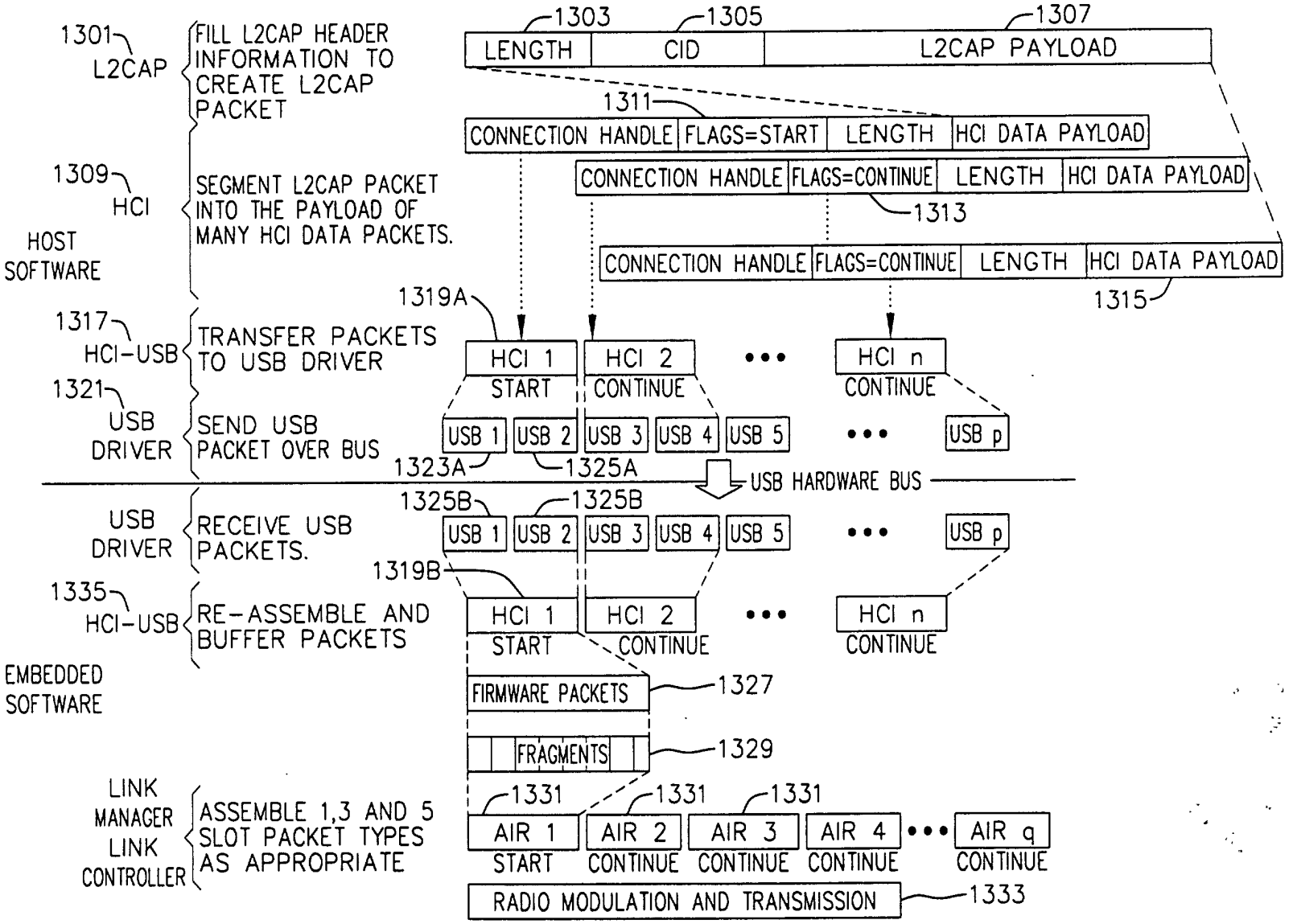

1203
1205
1206
1
0
LENGTH
BYTE 0
1
0
BYTE 1
L_CH
1207
1209
BYTE 63
1211
1213
0
0
FIRMWARE PACKET 1201
1215
1217
1219
0
1
1221

FIG. 13



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Application No. 09/788,061
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FIG. 14

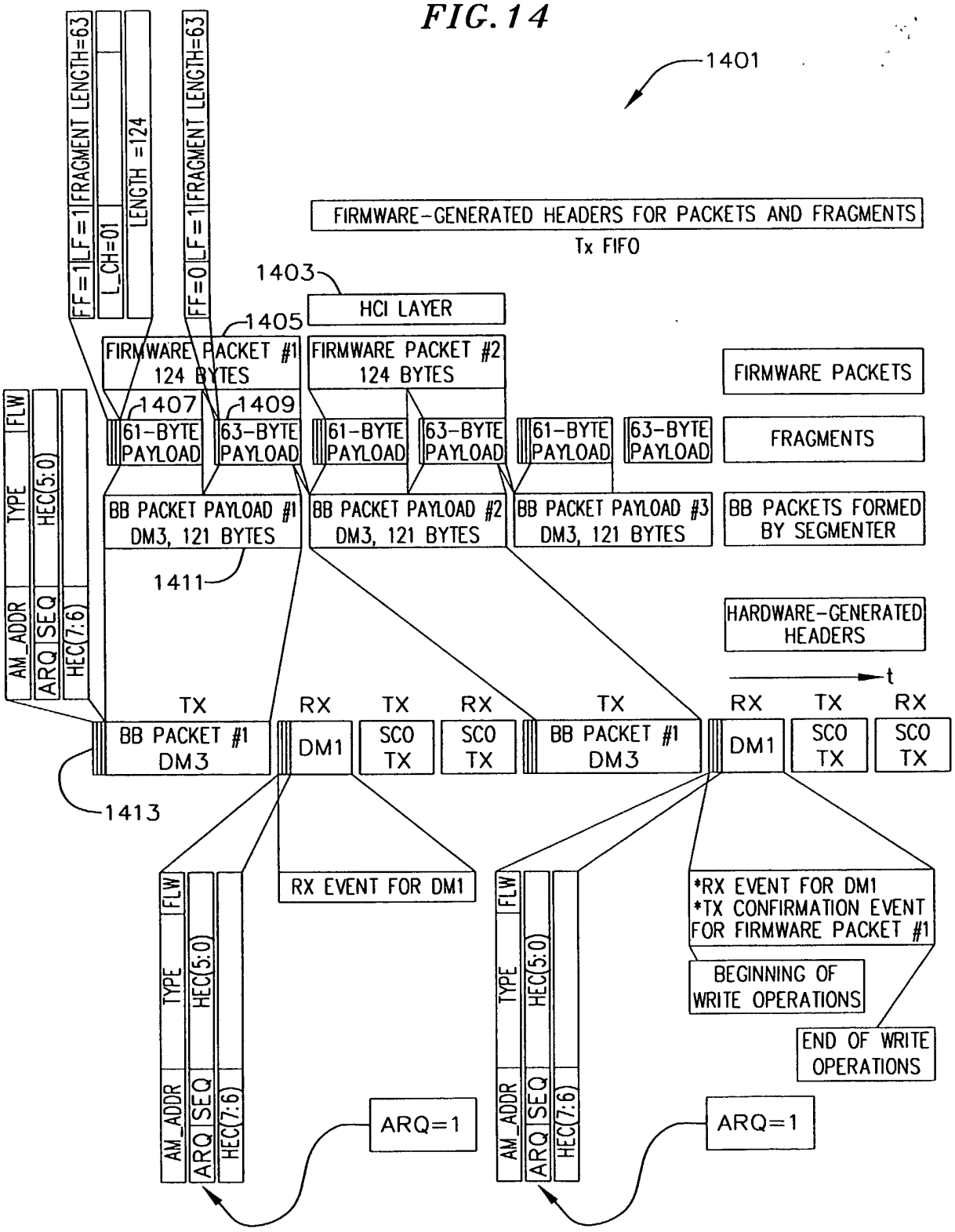

1401
FIRMWARE-GENERATED HEADERS FOR PACKETS AND FRAGMENTS
Tx FIFO
1403
HCI LAYER
1405
FIRMWARE PACKET #1
124 BYTES
FIRMWARE PACKET #2
124 BYTES
FIRMWARE PACKETS
1407
1409
61-BYTE PAYLOAD
63-BYTE PAYLOAD
61-BYTE PAYLOAD
63-BYTE PAYLOAD
61-BYTE PAYLOAD
63-BYTE PAYLOAD
FRAGMENTS
BB PACKET PAYLOAD #1
DM3, 121 BYTES
BB PACKET PAYLOAD #2
DM3, 121 BYTES
BB PACKET PAYLOAD #3
DM3, 121 BYTES
BB PACKETS FORMED BY SEGMENTER
1411
HARDWARE-GENERATED HEADERS
t
TX
RX
TX
RX
TX
RX
TX
SCO TX
BB PACKET #1
DM3
DM1
SCO TX
SCO TX
BB PACKET #1
DM3
DM1
SCO TX
SCO TX
1413
FF=1 LF=1 FRAGMENT LENGTH=63
L_CH=01
LENGTH =124
FF=0 LF=1 FRAGMENT LENGTH=63
FLW
TYPE
HEC(5:0)
AM_ADDR
ARQ SEQ
HEC(7:6)
RX EVENT FOR DM1
*RX EVENT FOR DM1
*TX CONFIRMATION EVENT
FOR FIRMWARE PACKET #1
BEGINNING OF WRITE OPERATIONS
END OF WRITE OPERATIONS
ARQ=1
ARQ=1

FIG. 15

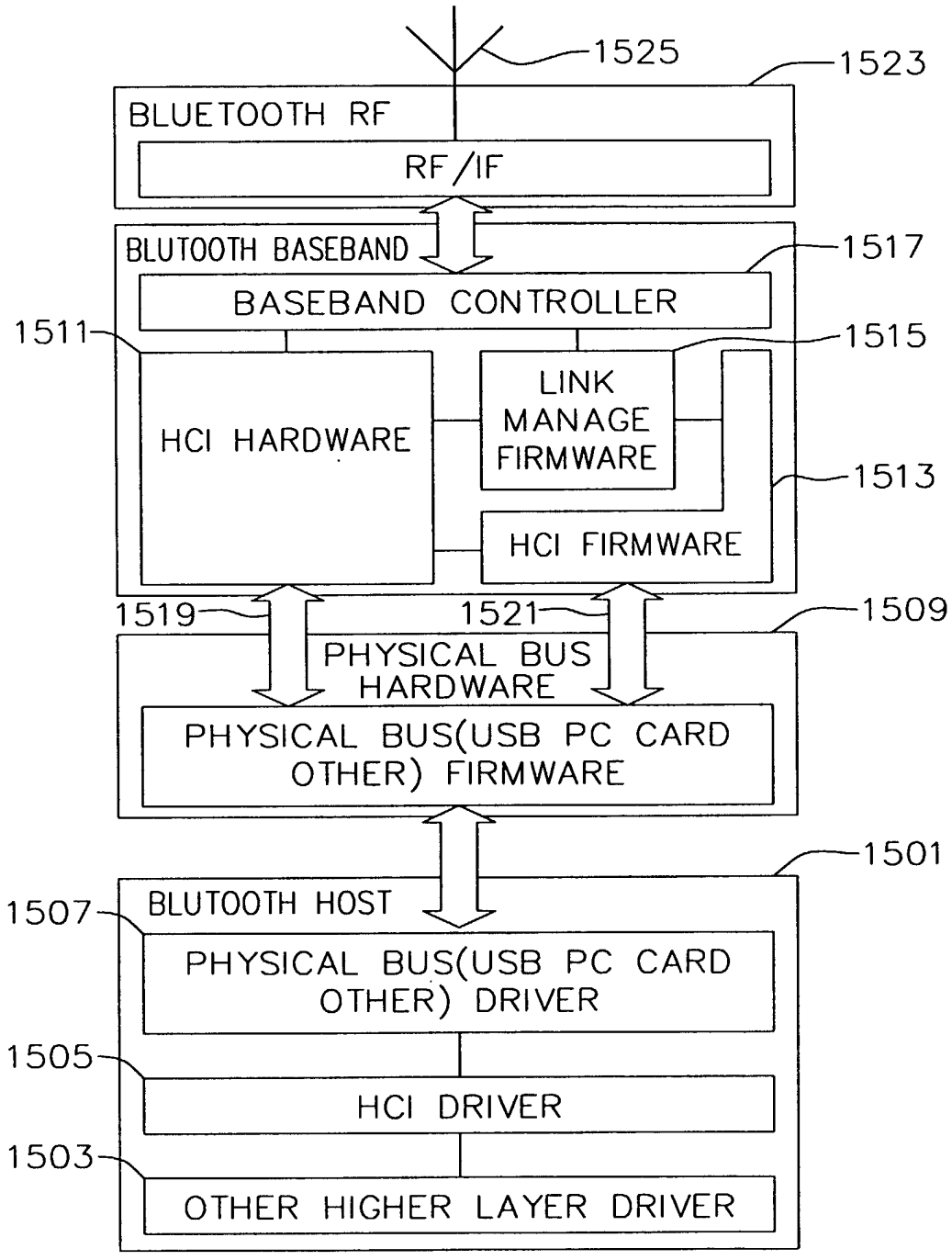

1525
1523
BLUETOOTH RF
RF/IF
BLUTOOTH BASEBAND
1517
BASEBAND CONTROLLER
1511
1515
HCI HARDWARE
LINK MANAGE FIRMWARE
1513
HCI FIRMWARE
1519
1521
1509
PHYSICAL BUS HARDWARE
PHYSICAL BUS(USB PC CARD OTHER) FIRMWARE
1501
1507
BLUTOOTH HOST
PHYSICAL BUS(USB PC CARD OTHER) DRIVER
1505
HCI DRIVER
1503
OTHER HIGHER LAYER DRIVER

FIG. 16

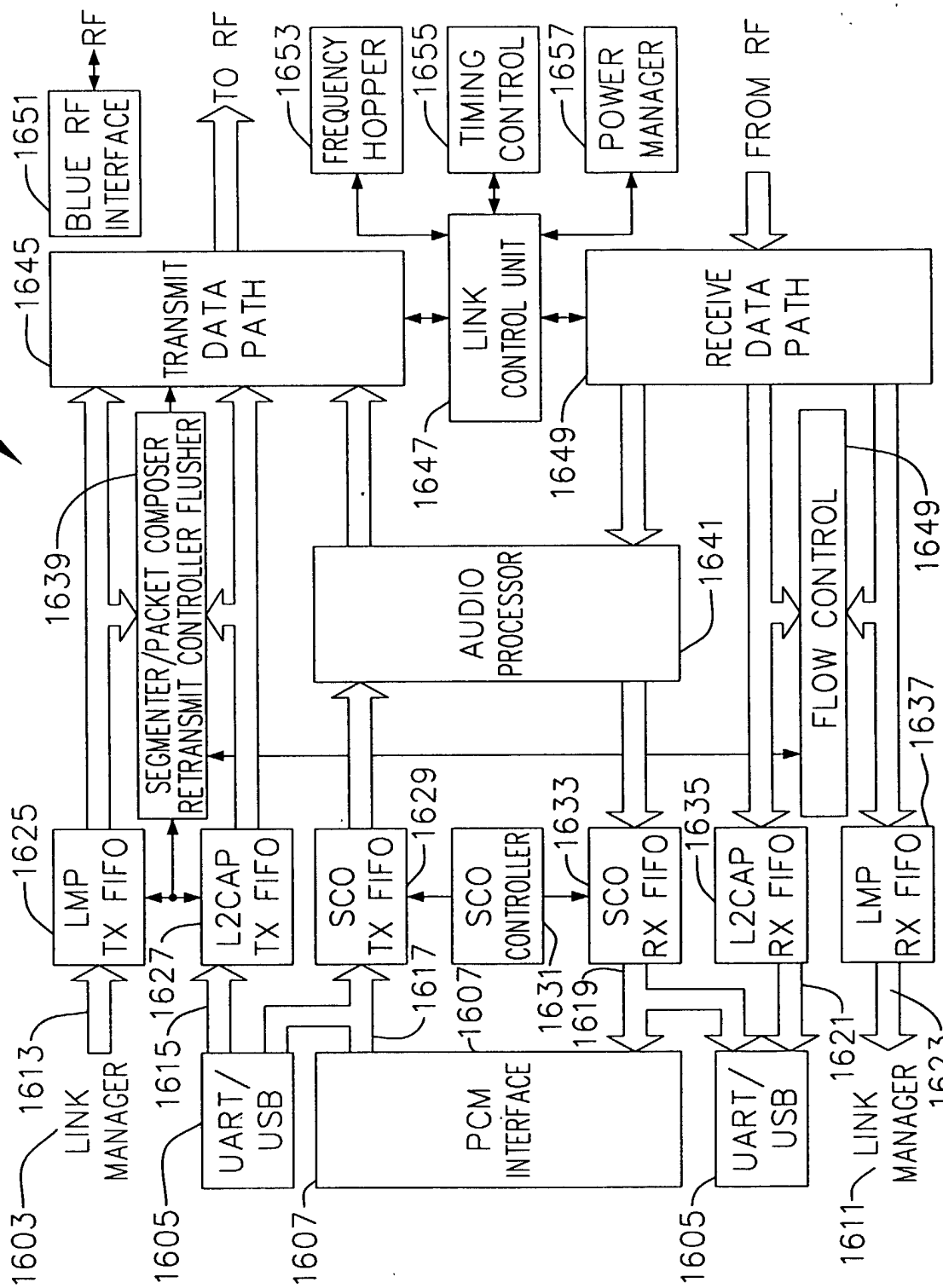
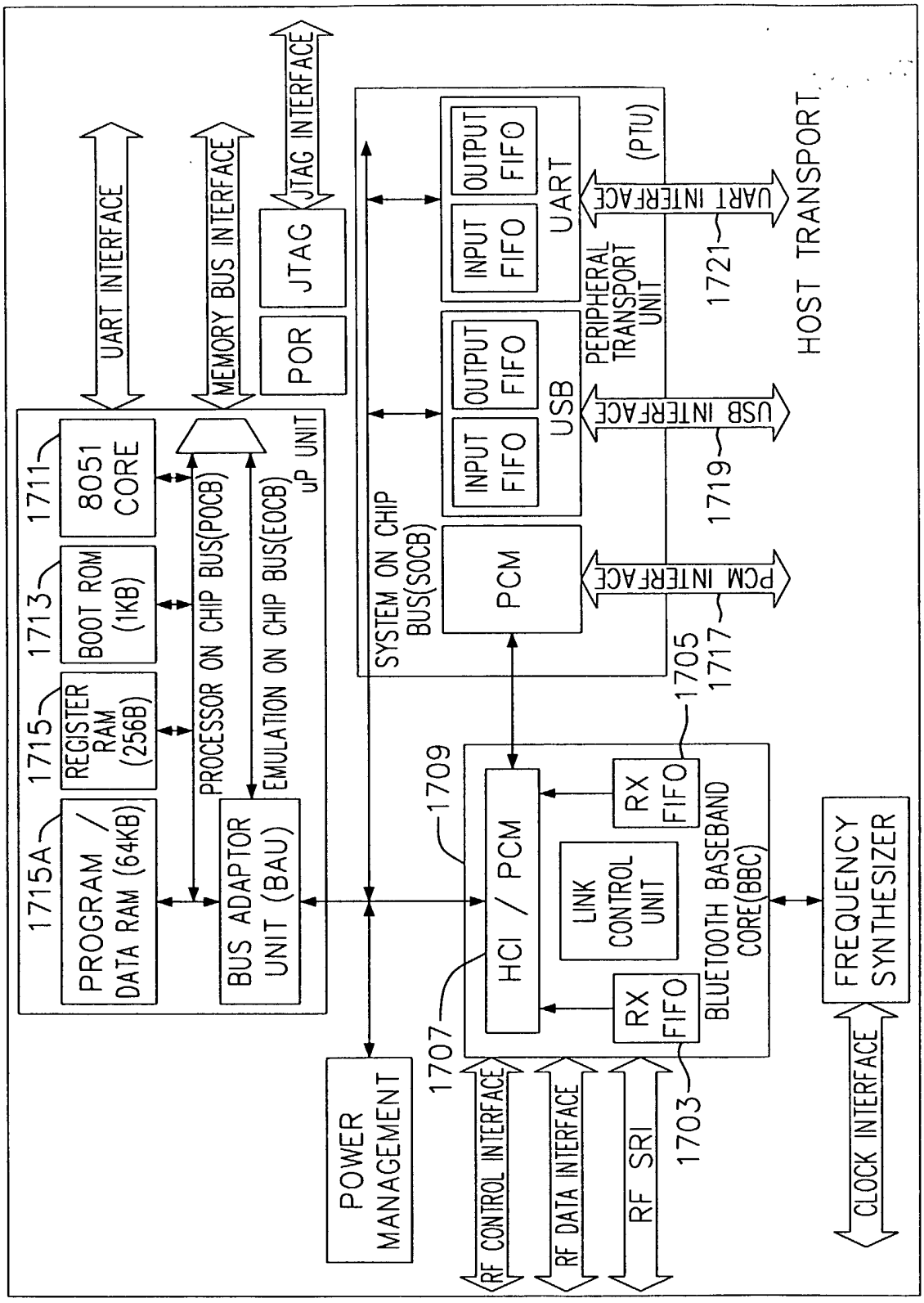

1601
RF
1651
BLUE RF INTERFACE
TO RF
1653
FREQUENCY HOPPER
1655
TIMING CONTROL
1657
POWER MANAGER
FROM RF
1645
TRANSMIT DATA PATH
LINK CONTROL UNIT
RECEIVE DATA PATH
1647
1649
1639
SEGMENTER/PACKET COMPOSER RETRANSMIT CONTROLLER FLUSHER
AUDIO PROCESSOR
1641
FLOW CONTROL
1649
1625
LMP TX FIFO
L2CAP TX FIFO
SCO TX FIFO
1629
SCO CONTROLLER
1633
SCO RX FIFO
1635
L2CAP RX FIFO
LMP RX FIFO
1637
1613
1615
1627
1617
1607
1631
1619
1621
1623
LINK MANAGER
UART/ USB
PCM INTERFACE
UART/ USB
LINK MANAGER
1603
1605
1607
1605
1611

FIG. 17


1701
UART INTERFACE
MEMORY BUS INTERFACE
JTAG INTERFACE
POR
JTAG
8051 CORE
1711
BOOT ROM (1KB)
1713
REGISTER RAM (256B)
1715
PROGRAM / DATA RAM (64KB)
1715A
PROCESSOR ON CHIP BUS(POCB)
EMULATION ON CHIP BUS(EOCB)
BUS ADAPTOR UNIT (BAU)
uP UNIT
SYSTEM ON CHIP BUS(SOCB)
PCM
INPUT FIFO
OUTPUT FIFO
USB
UART
PERIPHERAL TRANSPORT UNIT (PTU)
HOST TRANSPORT
UART INTERFACE
USB INTERFACE
PCM INTERFACE
1721
1719
1717
1705
1709
HCI / PCM
LINK CONTROL UNIT
RX FIFO
RX FIFO
BLUETOOTH BASEBAND CORE(BBC)
1707
1703
POWER MANAGEMENT
FREQUENCY SYNTHESIZER
RF CONTROL INTERFACE
RF DATA INTERFACE
RF SRI
CLOCK INTERFACE

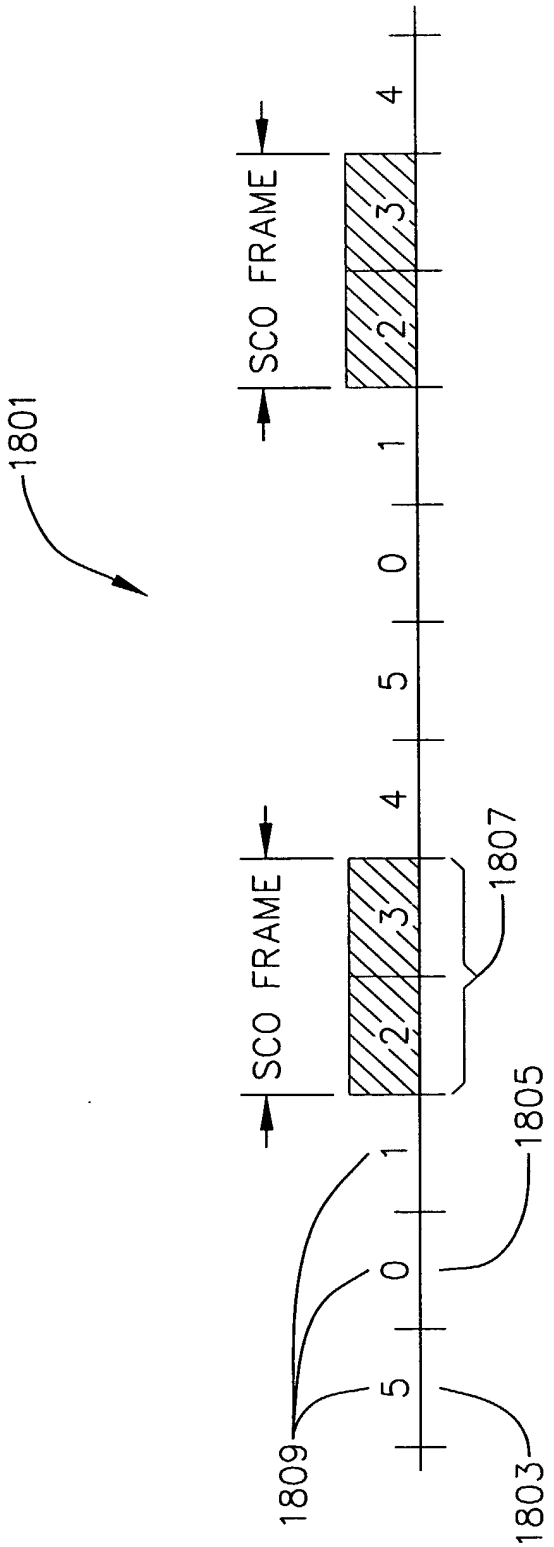


FIG. 18

FIG. 19A

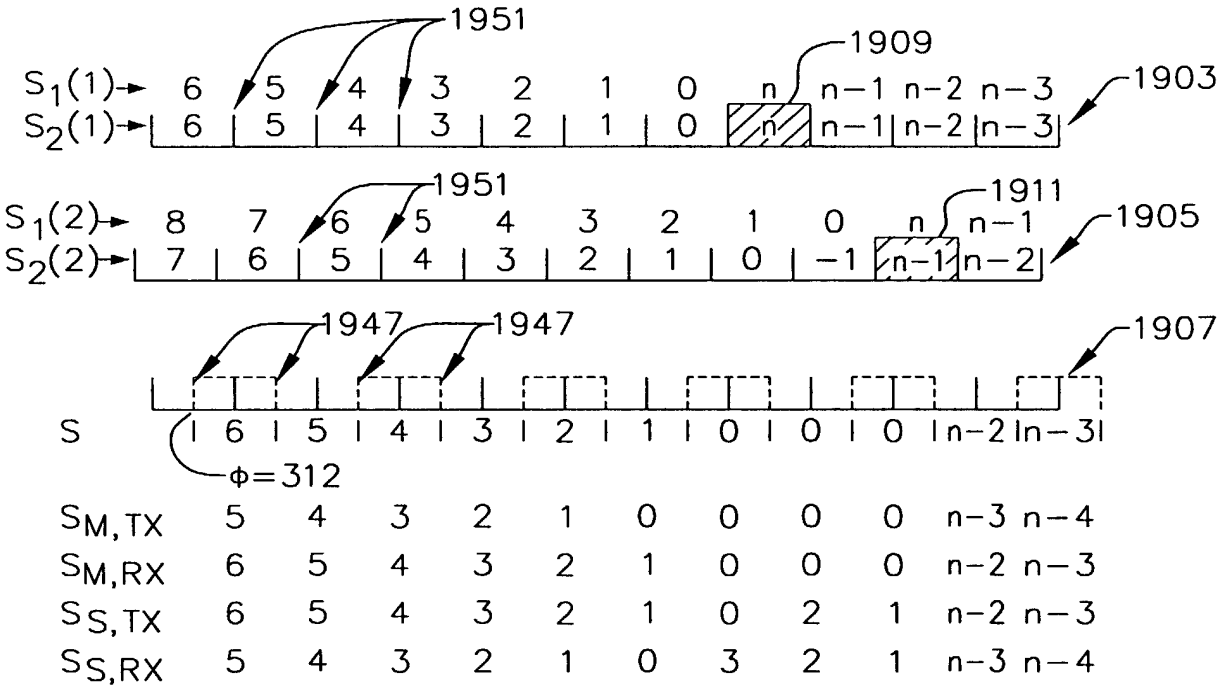


FIG. 19B

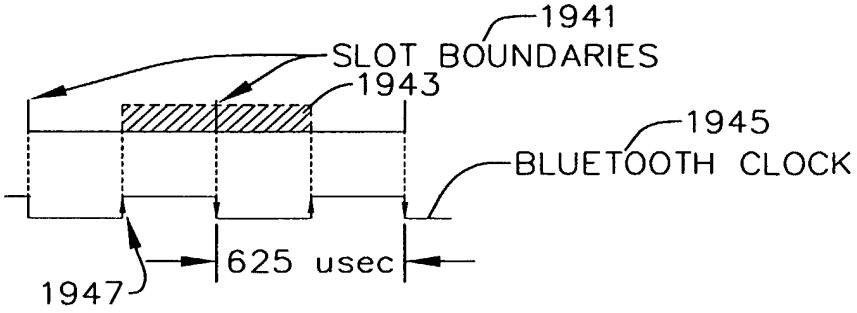


FIG.20

TABLE 1. PACKET TYPE PRIORITY

2001

RANGE LABEL	MIN BYTES IN BUFFER	MAX BYTES IN BUFFER	1ST. CHOICE	2ND. CHOICE	3RD. CHOICE	4TH. CHOICE	5TH. CHOICE	6TH. CHOICE
a	0	0	NULL	NULL	NULL	NULL	NULL	NULL
b	1	17	DM1	DH1	DM3	DH3	DM5	DH5
c	18	27	DH1	DM3	DH3	DM5	DH5	DM1
d	28	121	DM3	DH3	DM5	DH5	DH1	DM1
e	122	183	DH3	DM5	DH5	DM3	DH1	DM1
f	184	224	DM5	DH5	DH3	DM3	DH1	DM1
g	225	339	DH5	DM5	DH3	DM3	DH1	DM1
h	339		DH5	DM5	DH3	DM3	DH1	DM1

FIG.21

EXAMPLE OF A FRAGMENT CHOOSER FOR 16 FRAGMENTS, N=4
(FOR 127 FRAGMENTS N=7)

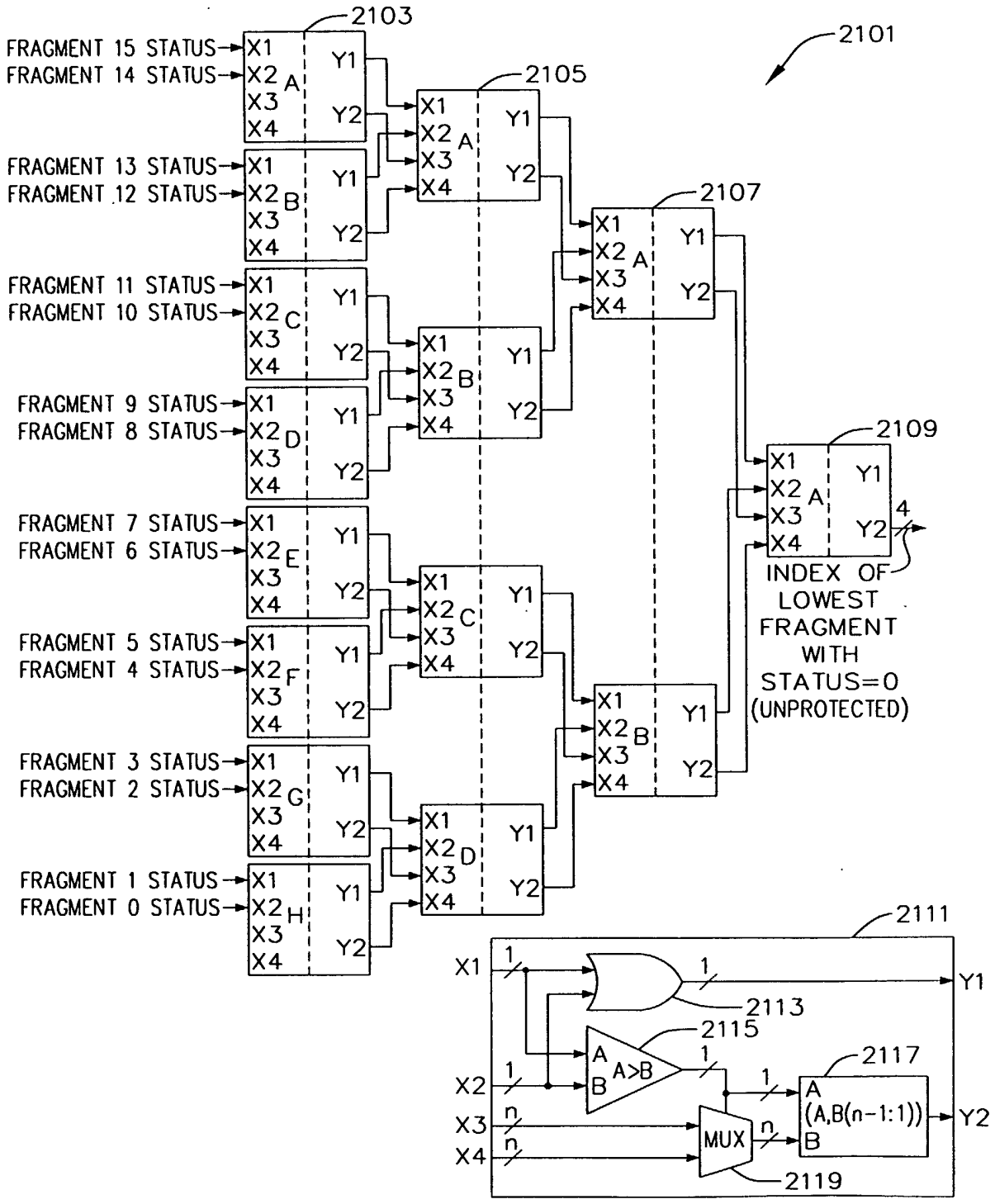


FIG. 22

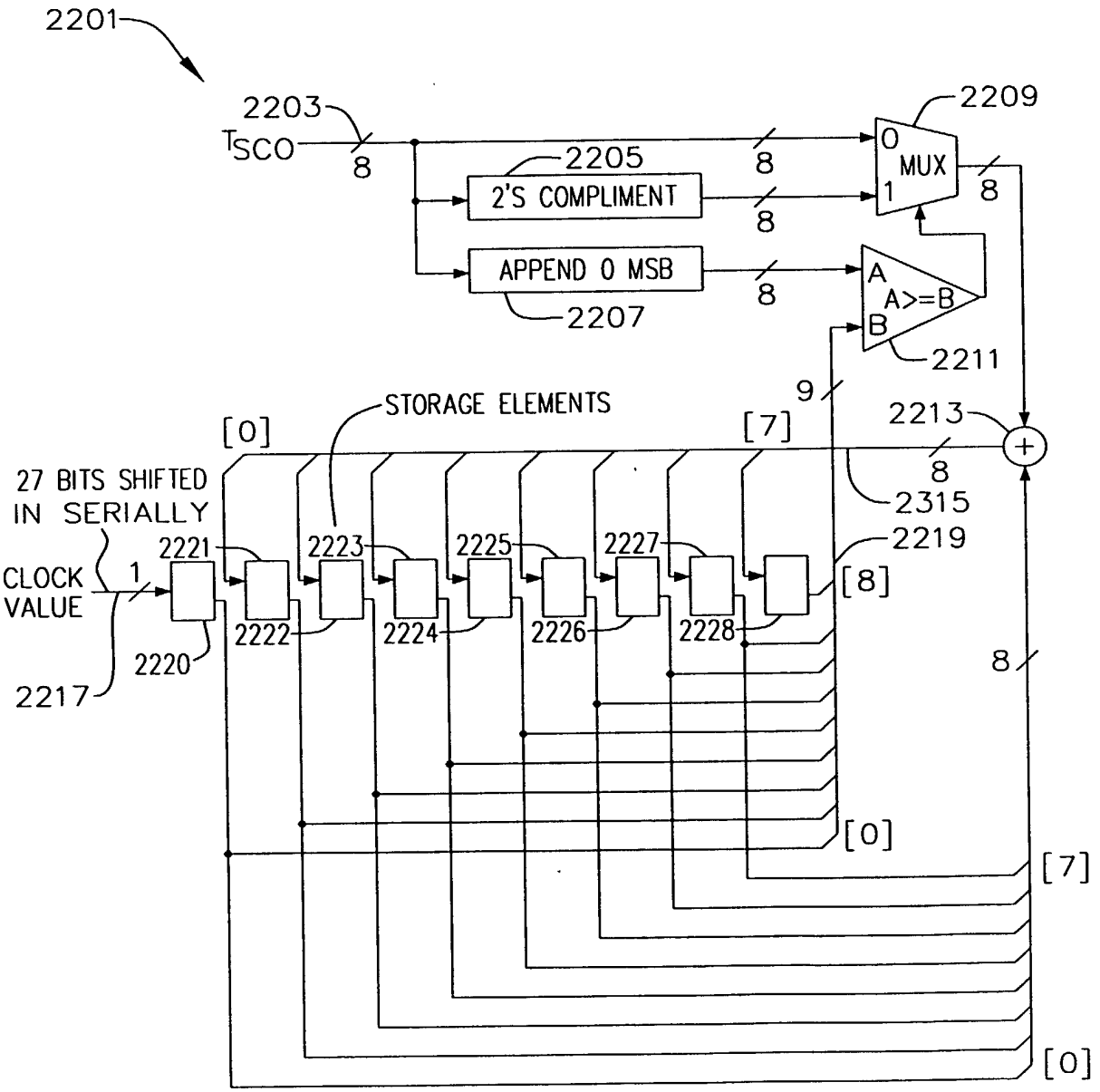

CIRCUIT TO CALCULATE CLK MOD Y, WHERE CLK IS 27 BITS AND T IS 8 BITS
2201
2203
TSCO
8
2205
2'S COMPLIMENT
APPEND 0 MSB
2207
2209
0
MUX
1
A
A>=B
B
2211
9
2213
+
STORAGE ELEMENTS
[0]
[7]
27 BITS SHIFTED IN SERIALLY
CLOCK VALUE
1
2217
2220
2221
2222
2223
2224
2225
2226
2227
2228
2219
[8]
2315
[0]
[7]
[0]

FIG.23

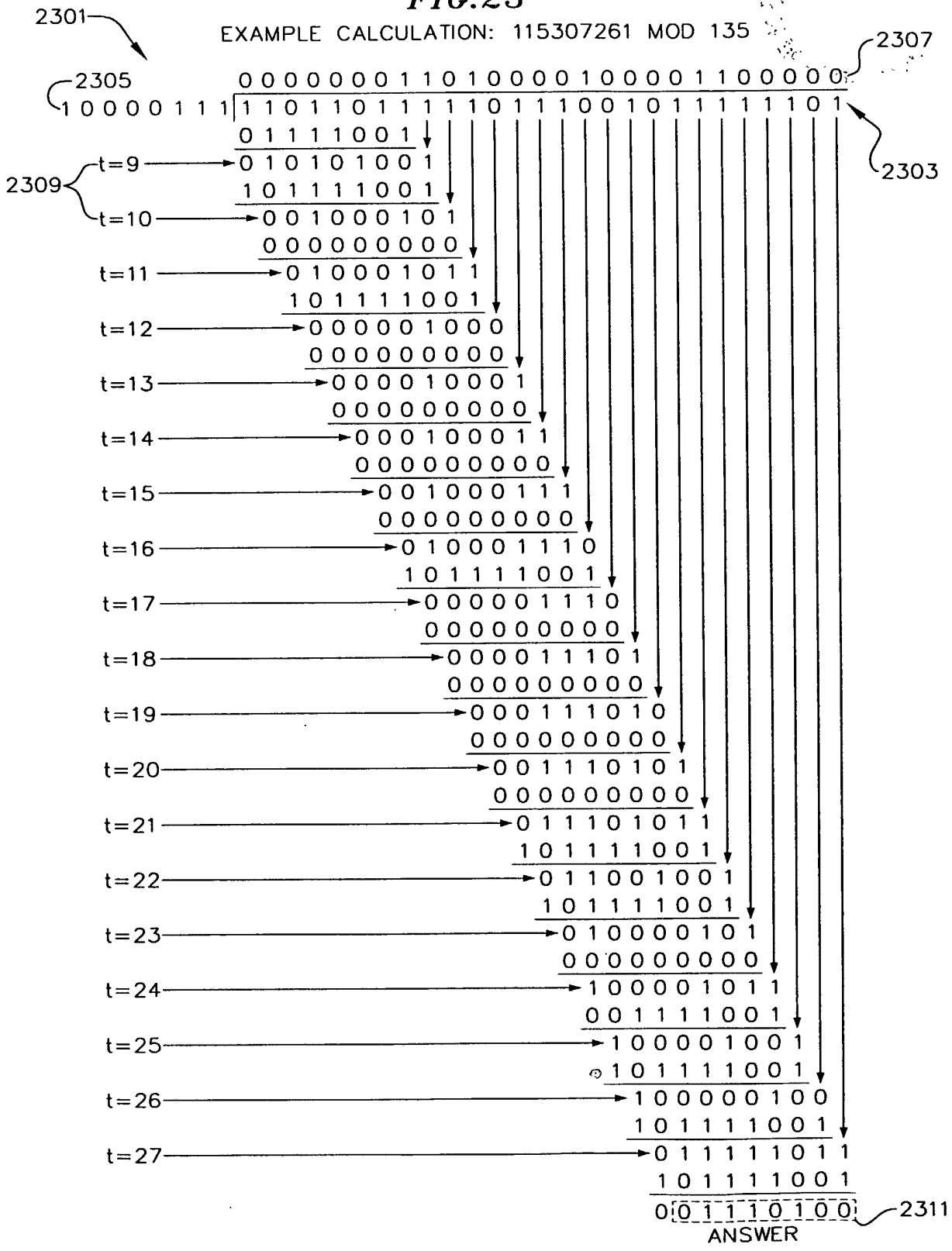

2301
EXAMPLE CALCULATION: 115307261 MOD 135
2307
2305
0 0 0 0 0 0 0 1 1 0 1 0 0 0 0 1 0 0 0 0 1 1 0 0 0 0 0
1 0 0 0 0 1 1 1 | 1 1 0 1 1 0 1 1 1 1 1 0 1 1 1 0 0 1 0 1 1 1 1 1 1 0 1
2303
0 1 1 1 1 0 0 1
2309
t=9
0 1 0 1 0 1 0 0 1
1 0 1 1 1 1 0 0 1
t=10
0 0 1 0 0 0 1 0 1
0 0 0 0 0 0 0 0 0
t=11
0 1 0 0 0 1 0 1 1
1 0 1 1 1 1 0 0 1
t=12
0 0 0 0 0 1 0 0 0
0 0 0 0 0 0 0 0 0
t=13
0 0 0 0 1 0 0 0 1
0 0 0 0 0 0 0 0 0
t=14
0 0 0 1 0 0 0 1 1
0 0 0 0 0 0 0 0 0
t=15
0 0 1 0 0 0 1 1 1
0 0 0 0 0 0 0 0 0
t=16
0 1 0 0 0 1 1 1 0
1 0 1 1 1 1 0 0 1
t=17
0 0 0 0 0 1 1 1 0
0 0 0 0 0 0 0 0 0
t=18
0 0 0 0 1 1 1 0 1
0 0 0 0 0 0 0 0 0
t=19
0 0 0 1 1 1 0 1 0
0 0 0 0 0 0 0 0 0
t=20
0 0 1 1 1 0 1 0 1
0 0 0 0 0 0 0 0 0
t=21
0 1 1 1 0 1 0 1 1
1 0 1 1 1 1 0 0 1
t=22
0 1 1 0 0 1 0 0 1
1 0 1 1 1 1 0 0 1
t=23
0 1 0 0 0 0 1 0 1
0 0 0 0 0 0 0 0 0
t=24
1 0 0 0 0 1 0 1 1
0 0 1 1 1 1 0 0 1
t=25
1 0 0 0 0 1 0 0 1
1 0 1 1 1 1 0 0 1
t=26
1 0 0 0 0 0 1 0 0
1 0 1 1 1 1 0 0 1
t=27
0 1 1 1 1 1 0 1 1
1 0 1 1 1 1 0 0 1
0 0 1 1 1 0 1 0 0
2311
ANSWER

FIG.24

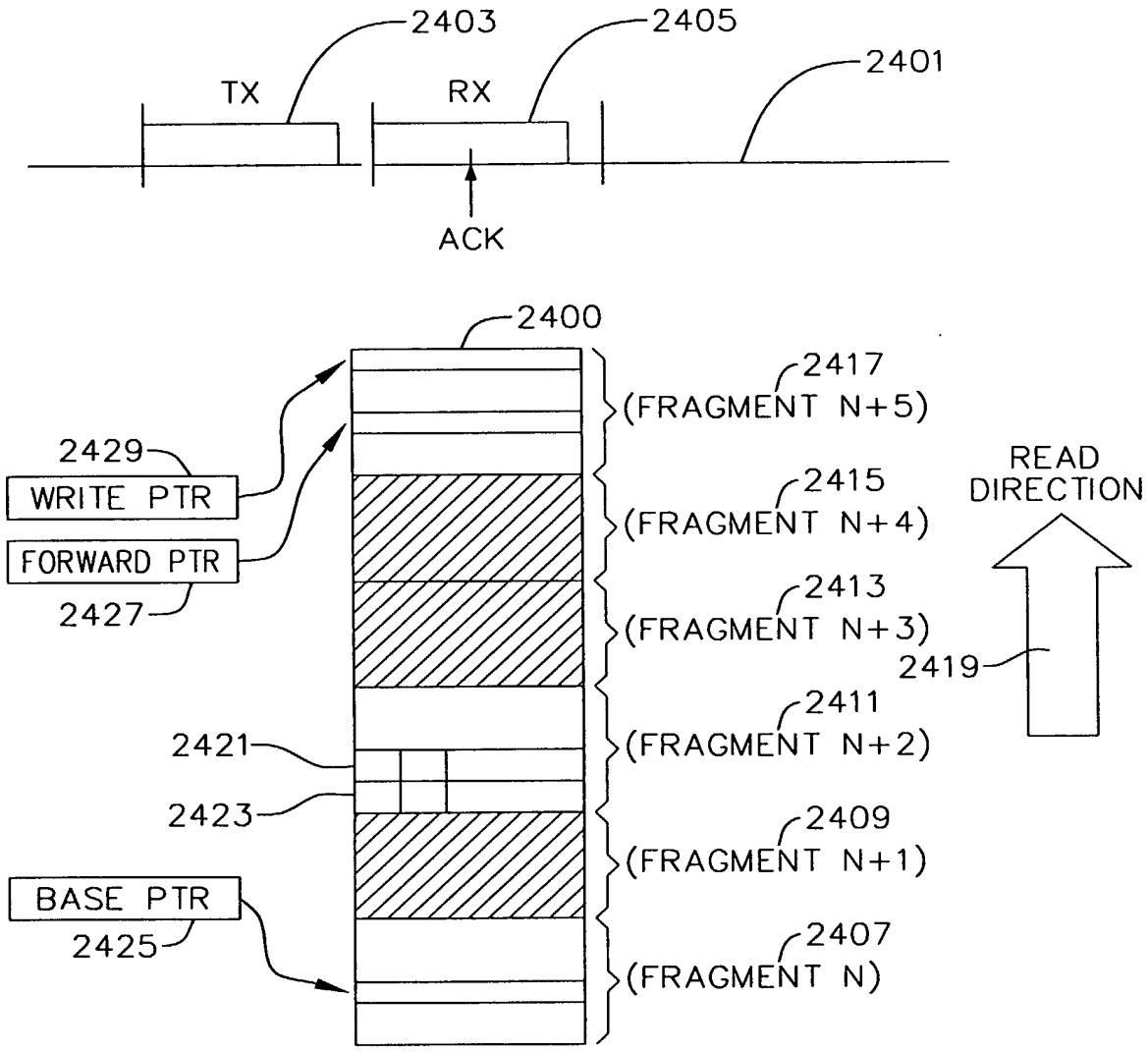

2403
2405
2401
TX
RX
ACK
2400
2417
(FRAGMENT N+5)
2429
WRITE PTR
2415
(FRAGMENT N+4)
READ
DIRECTION
FORWARD PTR
2427
2413
(FRAGMENT N+3)
2419
2411
(FRAGMENT N+2)
2421
2423
2409
(FRAGMENT N+1)
BASE PTR
2425
2407
(FRAGMENT N)

FIG.25

THE FOLLOWING DIPICTS THE BYTE GAUGE STATE MACHINE IN FLOW DIAGRAM FORM. NUMBERS IN PARENTHESES INDICATE THE STATE.

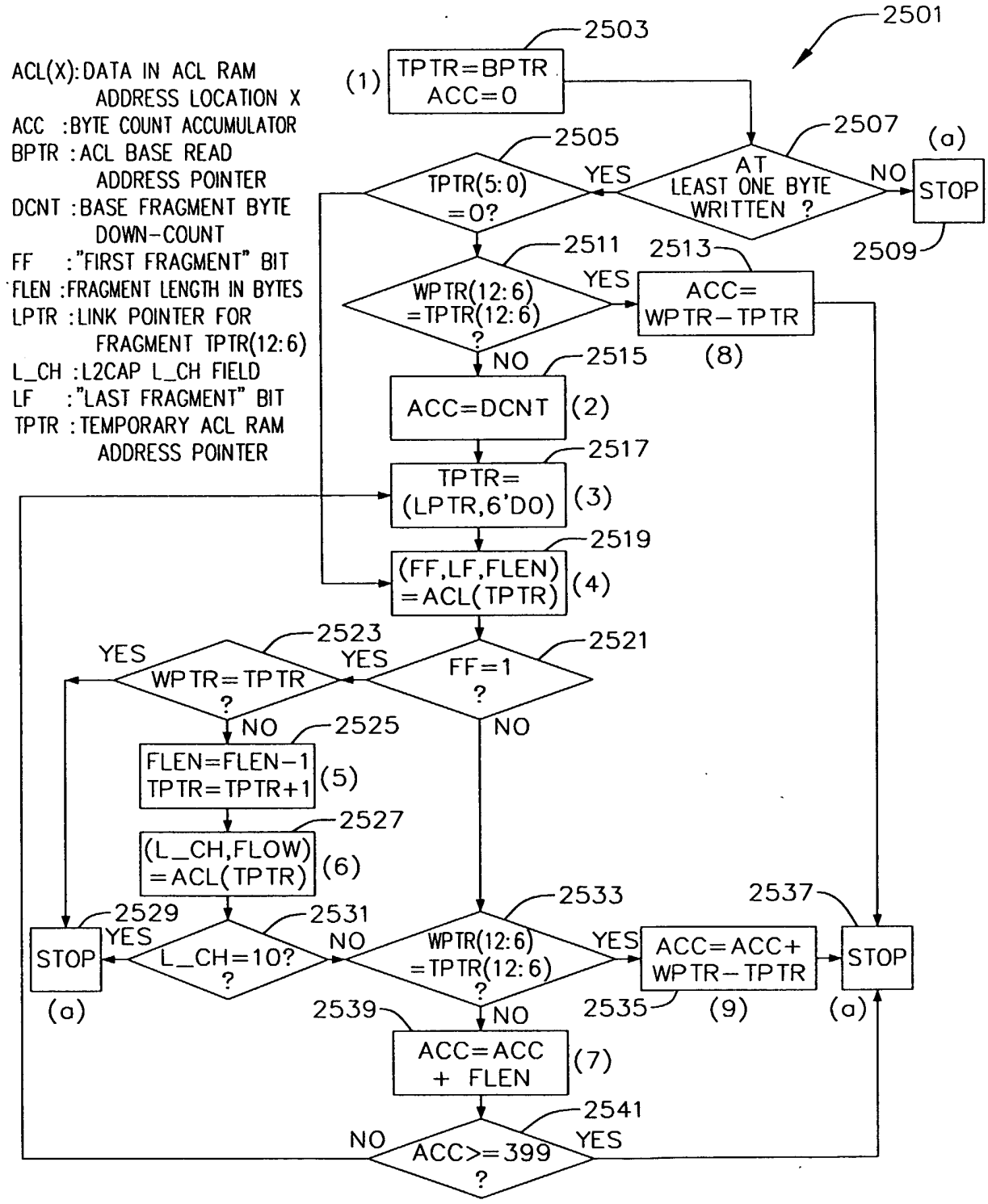
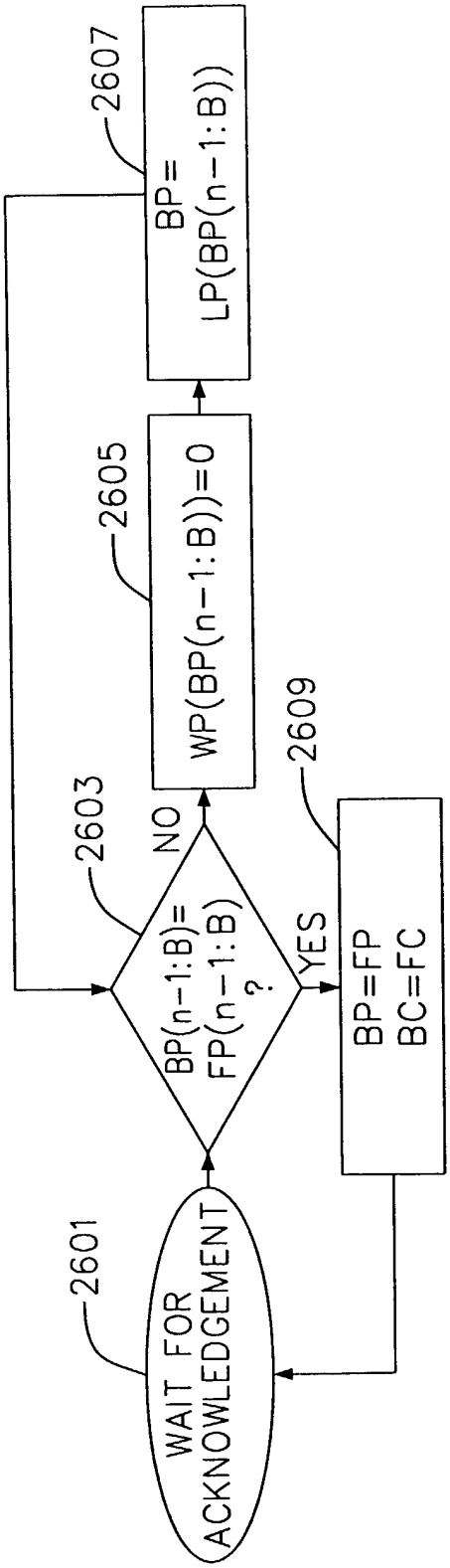


FIG.26

L2CAP PACKET FLUSH STATE MACHINE



KEY:

BBH1 : BASEBAND PACKET HEADER, 1ST. BYTE
BBH2 : BASEBAND PACKET HEADER, 2ND. BYTE
BC : BASE DOWN-COUNT (COUNTS DOWN FROM FRAGMENT LENGTH)
BP : BASE POINTER
FC : FORWARD DOWN-COUNT (COUNTS DOWN FROM FRAGMENT LENGTH)
FP : FORWARD POINTER
LP : LINK POINTER ARRAY
MEM : L2CAP MEMORY ARRAY
N : NUMBER OF BITS IN ADDRESS TO MEMORY ARRAY
PB : PAYLOAD BYTE DOWN-COUNT (COUNTS DOWN FROM PACKET LENGTH)
PLH1 : PAYLOAD HEADER, 1ST. BYTE
PLH2 : PAYLOAD HEADER, 2ND. BYTE
WP : WRITE PROTECTION ARRAY --ONE BIT PER FRAGMENT

NOTATION:

-- : DECREMENT BY ONE
++ : INCREMENT BY ONE
X(Y) : ELEMENT Y OF ARRAY X
A(B:C) : BITS B THROUGH C OF N BIT BUS A
(D,E) : CONCATINATION OF D AND E
6'H : 6-BIT HEX VALUE

FIG.27

L2CAP PACKET TRANSMIT STATE MACHINE